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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/596,129	06/16/2000	Manfred Reithinger	00P7685US	2660

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EXAMINER	
CAO, PHAT X	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 05/09/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/596,129	Applicant(s) REITHINGER ET AL.	
	Examiner Phat X. Cao	Art Unit 2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 February 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3 and 6-21* is/are pending in the application.

4a) Of the above claim(s) *8-10 and 14* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,6,7,16 and 18-20* is/are rejected.

7)☒ Claim(s) *11-13,15,17 and 21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *14* .
4) ☒ Interview Summary (PTO-413) Paper No(s). *16* .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. The Request for Continued Examination filed 2/19/03 in Paper No. 13 is acknowledged.

Election/Restriction

2. Newly submitted claims 10 and 14 are directed to an invention that is independent or distinct from the invention originally claimed for the following reasons: newly submitted claims are directed to a wafer having a fusible link connecting a bus disposed in one of the plurality of chips and a corresponding one of the plurality of electrical components. On the other hand, the original claims are directed to a wafer having a plurality of voltage generators and an electrical conductor elevated above the regions in the fractional portion of the wafer.

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 10 and 14 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Claim Objections

3. Claim 1 is objected to because of the following informalities: in claim 1, line 3, "the wafersuch" should be changed to "the wafer such" . Appropriate correction is required.

4. The numbering of claims is not in accordance with 37 CFR 1.126 which requires the original numbering of the claims to be preserved throughout the prosecution. When claims are

canceled, the remaining claims must not be renumbered. When new claims are presented, they must be numbered consecutively beginning with the number next following the highest numbered claims previously presented (whether entered or not).

In this case, because there is no claim 19, misnumbered new claims 20, 21 and 22 in the amendment B, filed 2/19/03, have been renumbered as 19, 20, and 21, respectively. Therefore, the dependency of these renumbered claims needs to be changed to the corresponding independent claims.

Claim Rejections - 35 USC § 112

5. Claims 3 and 19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

- in renumbered claim 19, line 1, "The semiconductor package recited in claim 19 [emphasis added]" is unclear.

- claim 3 is unclear because it depends on canceled claim 2.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1 and 6-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Saitou et al (US. 5,739,546).

Saitou (Figs. 1 and 2) discloses a semiconductor, comprising: a semiconductor wafer having a plurality of integrated circuit chips 2 thereon, such chips being separated by "scribe line" separating regions 3 in the wafer, such wafer having a plurality of electrical contact pads 10; a dielectric member 7 having an electrical conductor 8 thereon, such electrical conductor 8 being elevated above the separating regions 3 in the fractional portion of the wafer, such electrical conductor 8 being electrically connected to the plurality of electrical contact pads 10 to electrically interconnect such plurality of chips, portions of the dielectric member 7 with portions of the electrical conductor 8 thereon spanning the regions in the wafer; and a plurality of voltage generator integrated circuits, each one being associated with, and disposed adjacent to, a corresponding one of the chips 2 (column 3, lines 19-22).

8. Claims 1 and 6-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Morari et al (US. 5,696,404).

Morari (Figs. 2 and 5) discloses a semiconductor, comprising: a semiconductor wafer having a plurality of integrated circuit chips 2 thereon, such chips being separated by separating regions 11 in the wafer such wafer having a plurality of electrical contacts 6 and 7; a dielectric member 14 having the line bus 12 of electrical conductor 13 thereon (Fig. 5 and column 4, lines 11-20), such electrical conductor 13 or the bus line 12 being elevated above the regions in the

fractional portion of the wafer, such electrical conductor 13 or the line bus 12 being electrically connected to the plurality of electrical contacts 6 and 7 to electrically interconnect such plurality of chips, portions of the dielectric member 14 with portions of the electrical conductor 13 or the line bus 12 thereon spanning the regions in the wafer (see Fig. 2 and column 4, lines 11-20); and a plurality of voltage generators 3 and 4 including a plurality of different electrical components (Fig. 3B), each one being associated with, and disposed adjacent to, a corresponding one of the chips (column 3, lines 30-36).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 16, 18 and renumbered claim 20 (original claim 21) rejected under 35 U.S.C. 103(a) as being unpatentable over Saitou et al **or** Murari et al in view of Barth et al (US. 6,233,184).

Neither Saitou nor Murari discloses the semiconductor wafer being a semiconductor package.

However, Barth (Fig. 3f) teaches the forming of a semiconductor wafer as a chip scale package 72 for connecting the membrane electrical conductor 20 to the electrical interconnect of

the printed circuit board 74. Accordingly, it would have been obvious to connect the electrical conductor of Saitou or Murari to the printed circuit board for the purpose of providing a fully tested package in wafer processing, so that the need for final module test after dicing is eliminated and the time and cost for testing and packaging is saved, as taught by Barth (column 9, lines 64-67).

Allowable Subject Matter

11. Claims 11-13, 15, 17, and renumbered claim 21 (original claim 22) are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art of record fails to disclose all of the combination of the device structure as recited in the above claims, including the voltage generators being disposed in the separating region.

Response to Arguments

12. With respect to Murari, Applicant argues that the bus line 12 of the conductor 13 does not span the separating regions in the wafer.

The Examiner respectfully disagrees because Murari's Fig. 2 clearly discloses the bus line 12 of the conductor 13 extending in the horizontal direction and spanning over the separating regions 11 extending in the vertical direction.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phat X. Cao whose telephone number is (703) 308-4917. The Examiner can normally be reached on Monday through Thursday. If attempts to reach the Examiner by telephone are unsuccessfully, the Examiner's supervisor, Wael Fahmy, can be reached on (703) 308-4918.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 308-0956. Group 2800 fax number is (703) 308-7722 or (703) 308-7724.

PHAT X. CAO
PRIMARY EXAMINER

PC
May 2, 2003